Patent Search

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Abstract:

The invention relates to a hazard-resilient ARM processor incorporating a five-stage pipelined architecture—Instruction Fetch, Decode, Execute, Memory, and Write-Back—to enhance instruction throughput and processing efficiency. A dedicated hazard detection and mitigation unit dynamically resolves data, control, and structural hazards using data forwarding, pipeline stalling, and branch prediction. The processor is implemented using Verilog HDL and synthesized on FPGA for real-time validation. The design ensures accurate instruction execution, reduced latency, and low power consumption, making it suitable for embedded, industrial, and IoT systems. The invention provides a reliable and scalable ARM-based architecture capable of high-speed, hazard-free processing under dynamic operational conditions.

Complete Specification

Description:FIELD OF THE INVENTION

[001] The present invention relates to the field of digital electronics and embedded systems, more particularly to microprocessor architecture design and pipeline hazard management in ARM-based processors. The invention specifically concerns a hazard-resilient pipelined ARM processor architecture that enhances the speed, accuracy, and reliability of instruction execution through efficient detection, mitigation, and resolution of data, control, and structural hazards.

[002] The invention lies within the domain of hardware design and synthesis for embedded systems, and is particularly applicable to FPGA and ASIC implementations requiring high-speed, low-power, and real-time performance. The processor architecture of the present invention provides improved instruction throughput by integrating data forwarding, pipeline stalling, and branch prediction mechanisms, ensuring stable and optimized performance for automotive, industrial automation, and IoT applications.

[003] This invention thus pertains to the design and implementation of a synthesizable, hazard-resilient ARM processor pipeline, offering an efficient and scalable solution to overcome limitations in existing processor designs used in modern embedded systems.

BACKGROUND OF THE INVENTION

View Application Status

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